CBCS SCHEME

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17NT34

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
MOSFETs and Digital Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define MOSFET. Discuss the working of MOSFET with suitable schematical diagram. **(10 Marks)**

b. Write a short notes on second order effects in MOS. **(10 Marks)**

OR

2 a. What is JFET? Discuss the working of JFET with neat schematical diagram. **(10 Marks)**

b. Explain the characteristic curves of MOSFET. **(10 Marks)**

Module-2

3 a. Explain the voltage transfer characteristics and load curves for NMOS and PMOS transistors of the static CMOS inverter in detail. **(10 Marks)**

b. Explaining concept of AOI and OAI in complex logic circuits. **(10 Marks)**

OR

4 a. Define MUX and explain the concept of 2:1 and 4:1 multiplexer using transmission gates. **(10 Marks)**

b. Implement 2-input NAND and NOR gate using CMOS logic. **(10 Marks)**

Module-3

5 a. Define sequential circuits, mention the types and with neat diagram, explain the operation of CMOS SR latch using NOR gate. **(10 Marks)**

b. Discuss about level and edge triggering in detail with relevant diagrams. **(10 Marks)**

OR

6 a. Explain the operation of CMOS gated SR latch with neat diagram. **(10 Marks)**

b. Write short notes on CMOS Schmitt trigger and MUX based latch. **(10 Marks)**

Module-4

7 a. With neat schematical diagram, explain the working of serial in serial output shift register in detail. **(10 Marks)**

b. Write short notes on modulus-4 synchronous up counter and modulus synchronous down counter. **(10 Marks)**

OR

8 a. Explain the concept of Johnson counter with the aid of truth table and logic diagram in detail. **(10 Marks)**

b. Write a short notes on modulus-8 synchronous upcounter and modulus-8 synchronous down counter. **(10 Marks)**

Module-5

9 a. Design counter using finite state machine with truth table, state and logical diagram in detail. **(10 Marks)**

b. With block diagram and state diagram explain the concept of Moore machine model in detail. **(10 Marks)**

OR

10 a. Explain the 4-bit sequence detector with conceptual and state diagram in detail. **(10 Marks)**

b. With block diagram and state diagram explain the concepts of mealy machine model in detail. **(10 Marks)**

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